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(54) Sub power plane to provide EMC filtering for VLSI devices.

(57) Electromagnetic filtering for a VLSI device having multiple power input leads is realized by employing a sub-power plane which is physically separate from a main power distribution system on a circuit board. The sub-power plane is placed directly under a corresponding VLSI device. Decoupling capacitors are connected to the sub-power plane and, in turn, to each of the power input leads on the VLSI device. Power is supplied from the main power distribution system to the sub-power plane via a ferrite bead type filter.

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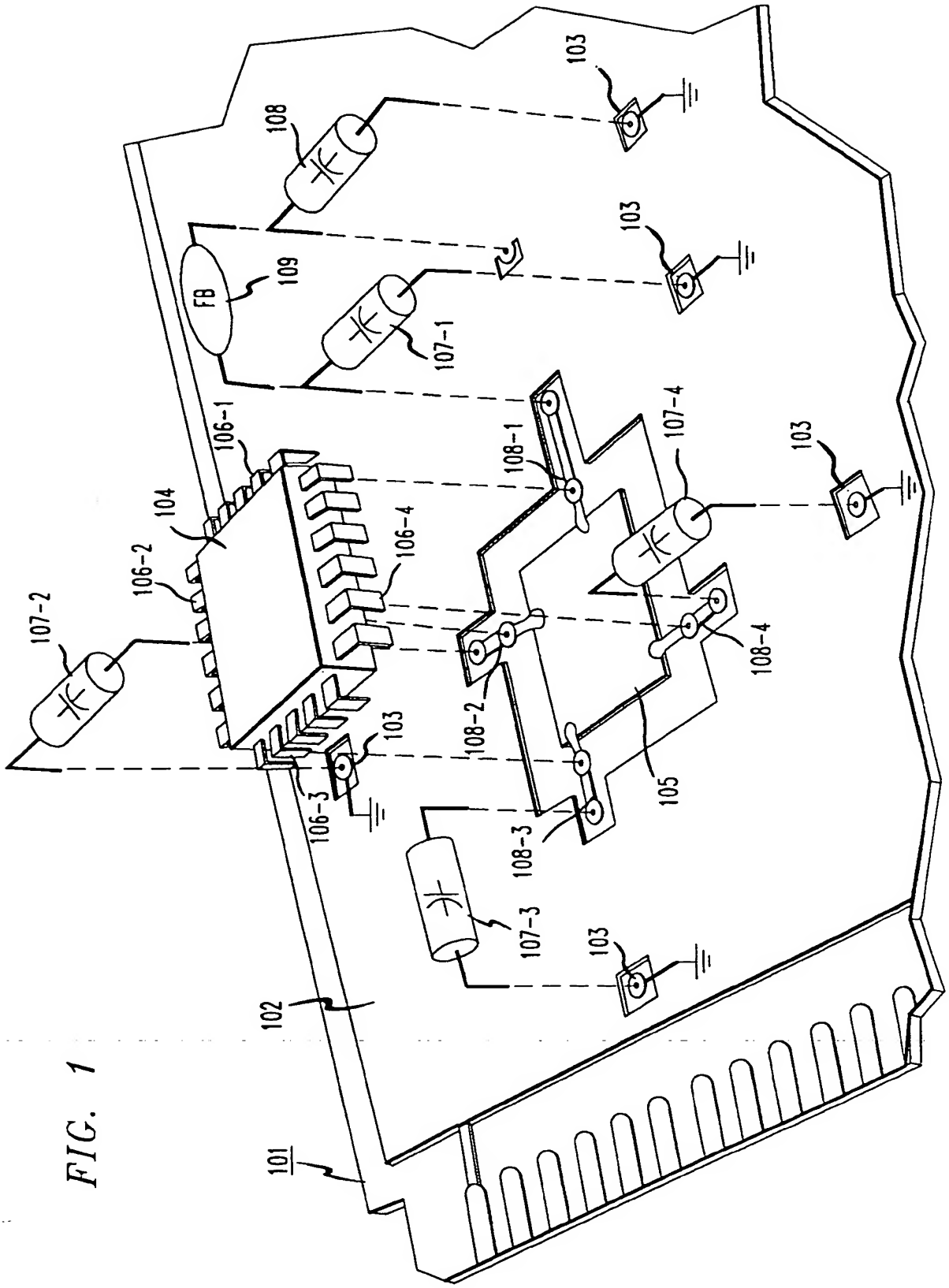


FIG. 1

T chnical Field

This invention relates to electromagnetic compatibility (EMC) and, more particularly, to power filtering for VLSI devices on a circuit board.

Background of the Invention

A problem with new VLSI devices having multiple power input leads is to provide a low impedance/low noise source of power to all of the power input leads. In the past, such VLSI devices were coupled directly to a main power plane or some other power distribution network, e.g., a grid. This power plane or grid typically covered the entire corresponding circuit board. Such arrangements could have "high" impedance or noise and, consequently, would cause so-called "glitches" on the output from the VLSI device. In turn, the VLSI device could induce noise on the power plane or power distribution network which caused problems with other devices on the circuit board. Additionally, so-called "common mode noise" would be mitted from the circuit board, which is highly undesirable. One attempt to eliminate the problems with the prior power distribution arrangements on circuit boards was to filter the power coming to the VLSI device and, then, employ a single power lead which was connected to all the power input leads on the VLSI d vice. A serious problem with this arrangement is that the single power lead is essentially an inductor at "high" frequencies which causes a significant amount of noise to be introduced into the VLSI device and also to be emitted from the board. Again, this is a highly undesirable condition.

Summary of the Invention

The problems with prior power distribution systems for VLSI devices having multiple power inputs ar ov rcome, in accordance with the invention, by employing a so-called "sub-power plane" in prescribed spatial relationship and physically separated from a main power distribution system on a circuit board. The sub-power plane is advantageously positioned on a circuit board to be directly under at least one corresponding VLSI device. Power is supplied from the sub-power plane to each power input lead on the at least one VLSI device. Additionally, a decoupling capacitor is connected between each power input lead connection of the sub-power plane and a ground potential, e.g., a ground grid. The decoupling capacitors advantageously supply transient switching current to the at least one VLSI device. Power from the main power distribution system is supplied to the sub-power plane via a filter. In a specific embodiment of the invention, the filter comprises a ferrite bead, i.e., an inductor, and appropriate decoupling capacitors.

Brief Description of th Drawings

In the drawing:

FIG. 1 is a perspective of a portion of a circuit board illustrating an embodiment of the invention;

FIG. 2 is a schematic representation of the invention;

FIG. 3 shows a circuit board including a plurality of VLSI devices and incorporating the invention;

FIG. 4 is another perspective showing the relationship of a plurality of sub-power planes to the main power plane and ground grid of a circuit board; and

FIG. 5 shows a portion of a circuit board including another embodiment of the invention.

Detailed Description

FIG. 1 shows a portion of a circuit board, including an embodiment of the invention. Accordingly, shown are circuit board 101 including main power distribution system 102, ground system 103, VLSI device 104 and sub-power plane 105. In this example, a solid main power plane is employed for power distribution system 102. It will be apparent to those skilled in the art that other power distribution systems, e.g., a power grid or the like, may equally be employed. Similarly, the ground system may be a grid, plane or the like. In this example, a ground grid is employed. VLSI device 104, which in this example has a plurality of power input leads 106-1 through 106-4, is intended to be placed directly over subpower plane 105. Power leads 106-1 through 106-4 are intended to be connected in circuit with sub-power plane 105 via connectors 108-1 through 108-4, respectively. Additionally, decoupling capacitors 107-1, 107-2, 107-3 and 107-4 are connected to sub-power plane 105 via connectors 108-1 through 108-4 and, hence, to power input leads 106-1 through 106-4, respectively. Capacitors 107 supply transient switching current to VLSI device 104, from sub-power plane 105. Although the illustration in FIG. 1 shows the capacitors as axial lead type, which are to be through mounted, in a preferred embodiment, surface mounted capacitors are employed. Since, VLSI device 104 for which the sub-power plane of this invention is to be employed are used for "high" frequency applications, for example, 25 MHz or above, the decoupling capacitors should be of a type used for such high frequency applications. A preferred type of capacitor is a ceramic type. The power from the main power plane 102 is supplied to sub-power plane 105 via a filter comprising capacitor 108, inductor 109 and decoupling capacitor 107-1, which is a familiar π type filter. Inductor 109, preferably is a so-called "ferrite bead" inductor of a type well known in the art. Although sub-power plane 105 is shown as being completely surrounded by main power plane 104, it will be apparent that it can be placed anywhere in rela-

tionship to the main power plane, even at the edge or a comer of circuit board 101. It is further noted that as shown in FIG. 1, sub-power plane 105 is in the same spatial planar relationship as main power plane 102 relaktive to the surface of circuit board 101. That is, sub-power plane 105 is in the same plane as the main power plane 102.

As illustrated in FIG. 1, the sub-power plane 105 is physically separated, i.e. decoupled from the main power plane, and situated directly below and essenbally contiguous with VLSI device 104. It is noted that sub-power plane 105 is a low impedance and, hence, low inductance source of power for all of the power leads 106 of VLSI device 104. The unique configuration of power plane 105 and capacitors 107-1 through 107-4, in this example, essentially form a distributed filter arrangement for the "high" frequency VLSI device. This unique configuration of sub-power plane 105 and capacitors 107 also provides the switching current at the extremely high speeds, for example, 1 nanosecond, required by high speed VLSI device 104 intended to be mounted on circuit board 101. Additionally, sub-power plane 105 in conjunction with capacitors 107, provides a localized radio frequ ncy counterpoise, i.e. ground plane, for the radio frequency fields radiated from the VLSI device 104, wh n operating at the high frequencies. Again, it is not d that these type VLSI devices are intended to operate in a range of 25 MHz and above. Thus, it is seen by using a π filter comprising capacitors 107-1 and 108 and ferrite bead 109 to couple power to sub-power plane 105 and decoupling capacitors 107 associated with each of the power leads 106 on the VLSI device 104, a unique power distribution and radiation suppression system is formed. A technical advantage of this unique power distribution system is that is minimizes electromagnetic radiation from the circuit board.

FIG. 2 illustrates in schematic diagram form the pow r distribution system illustrated in FIG. 1. Accordingly, the power from the main power plane 102 is supplied via decoupling capacitor 108 and ferrite bead 109 to decoupling capacitor 107-1 and to sub-power plane 105. Connected to power plane 105 are additional decoupling capacitors 107-2 through 107-4 and power input leads 106-1 through 106-4 of VLSI device 104. Additionally, capacitor 108, ferrite bead 109 and capacitor 107-1 form the well know π filter arrangement, as discussed above. The power supplied via main power plane 102 can be any desired voltage.

FIG. 3 shows circuit board 301 including a main power plane 102 and a plurality of VLSI devices each of which is mounted directly over a corresponding sub-power plane of this invention. Although the elements of each of the VLSI devices and its corresponding sub-power plane are arranged in similar fashion, only one VLSI device and sub-power plane have been numbered to correspond to the implementation of the invention as shown in FIG. 1.

FIG. 4 illustrates a preferred embodiment of the invention. Accordingly, shown are circuit board 401, a main power plane 402, a plurality of sub-power planes 403-1, 403-2 and 403-3. As noted above, sub-power planes 403 are in prescribed spatial relationships to the main power plane 402 and physically decoupled from it, as illustrated. FIG. 4 also shows that the prescribed spatial relationship of sub-power planes 403 is that the are in the same spatial planar relationship as main power plane 402 relative to the surface of circuit board 401. That is, sub-power planes 403 are in the same plane as main power-plane 402. Also, shown is pound grid 404, which is physically under and insulated from power plane 402 and sub-power planes 403, in known fashion.

FIG. 5 illustrates a portion of circuit board 501 and including another embodiment of the invention. Accordingly, shown are VLSI devices 501 and 502, which are connected to circuit board 500 over sub-power plane 503, shown in dashed outline. In this embodiment of the invention, a plurality of VLSI devices which are co-related in operation, can share the same sub-power plane 503. Such VLSI devices, for example, may comprise a microprocessor, i.e. device 501, and its associated clock or line driver circuitry, i.e. VLSI device 502. The decoupling and supplying of the power from the main power plane 504 are as described above in relationship to FIG. 1. The reason that a plurality of VLSI devices can be placed on a single sub-power plane is that devices with similar noise potential can be filtered using the same filter and sub-power plane arrangement. Such VLSI devices usually operate in conjunction with each other as a single entity-passing data among the VLSI devices.

Although this embodiment of the invention has been described for a circuit board including one power plane, it will be apparent to those skilled in the art that it is equally applicable to circuit boards having more than one main power plane.

Claims

1. A circuit board comprising:
   a ground system; and
   a main power distribution system; and being
   CHARACTERIZED BY
   at least one sub-power plane disposed in prescribed spatial relationship with and physically separate from said main power distribution system, said sub-power plane being adapted to be connected to at least one VLSI device having multiple power input leads.

2. A circuit board as defined in claim 1 CHARAC-

TERIZED BY said at least one sub-power plane being adapted to be connected directly under at least one corresponding VLSI device.

3. A circuit board as defined in claim 2 CHARACTERIZED BY a plurality of capacitors and CHARACTERIZED IN THAT said at least one sub-power plane is adapted to connect a first capacitor to a first power input lead of said VLSI device and to connect at least a second capacitor to a second power input lead of said VLSI device.

4. A circuit as defined in claim 2 CHARACTERIZED BY said sub-power plane being adapted to connect said plurality of capacitors to said multiple power input leads of said VLSI device on a one-to-one basis.

5. A circuit board as defined in claim 3 CHARACTERIZED BY a filter connecting said sub-power plane to said main power distribution systems for supplying power to said sub-power plane.

6. A circuit board as defined in claim 5 CHARACTERIZED IN THAT said filter comprises a capacitor, a ferrite bead and one of said plurality capacitors and is arranged in a π configuration.

7. A circuit board as defined in claim 6 CHARACTERIZED BY said ground system being a ground grid and each of said capacitors having a terminal adapted to be connected to said ground grid.

8. A circuit board as defined in claim 3 CHARACTERIZED IN THAT said main power distribution system is a main power plane having said at least one sub-power plane disposed therein and physically separated therefrom.

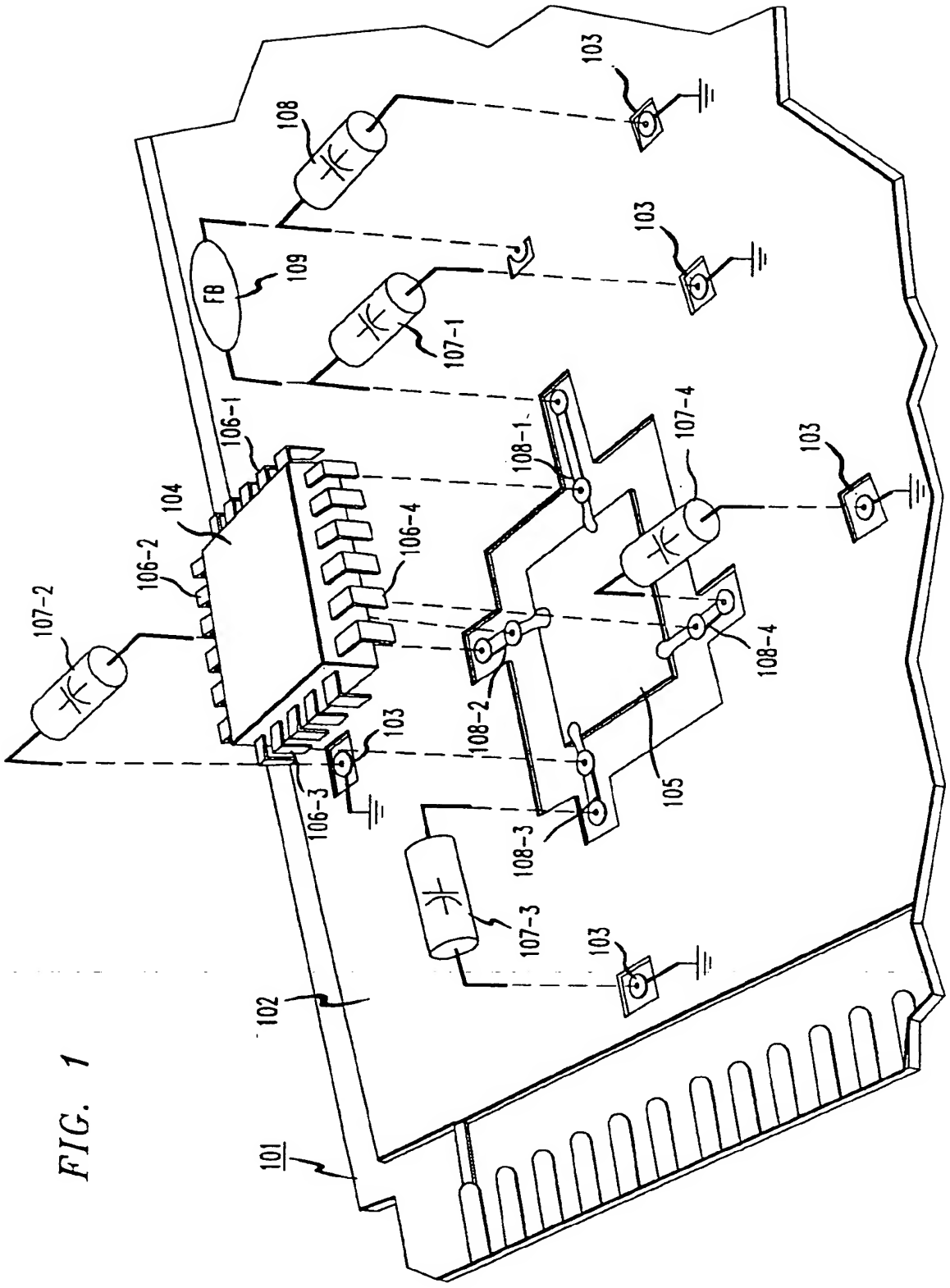
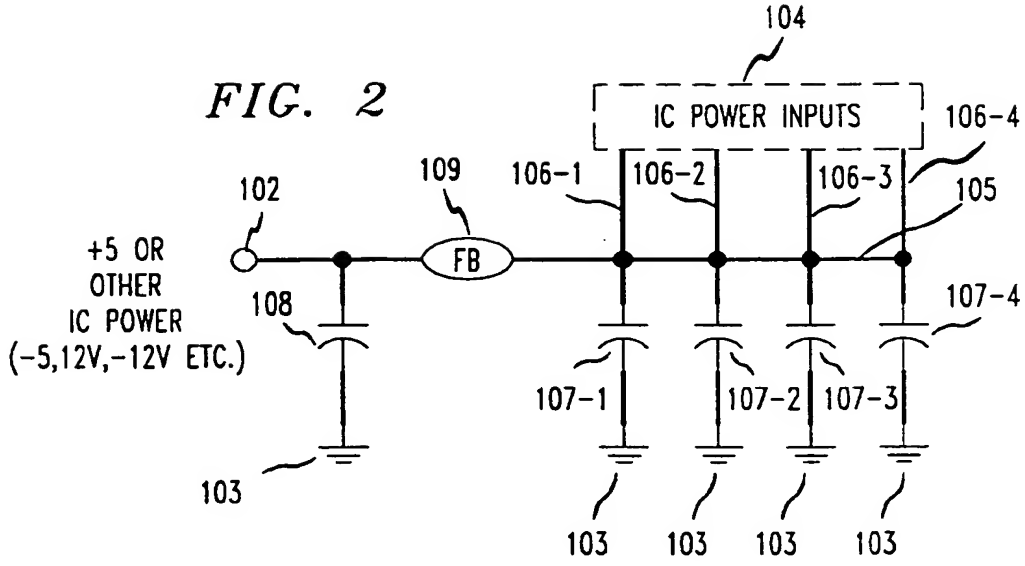


FIG. 1

FIG. 2



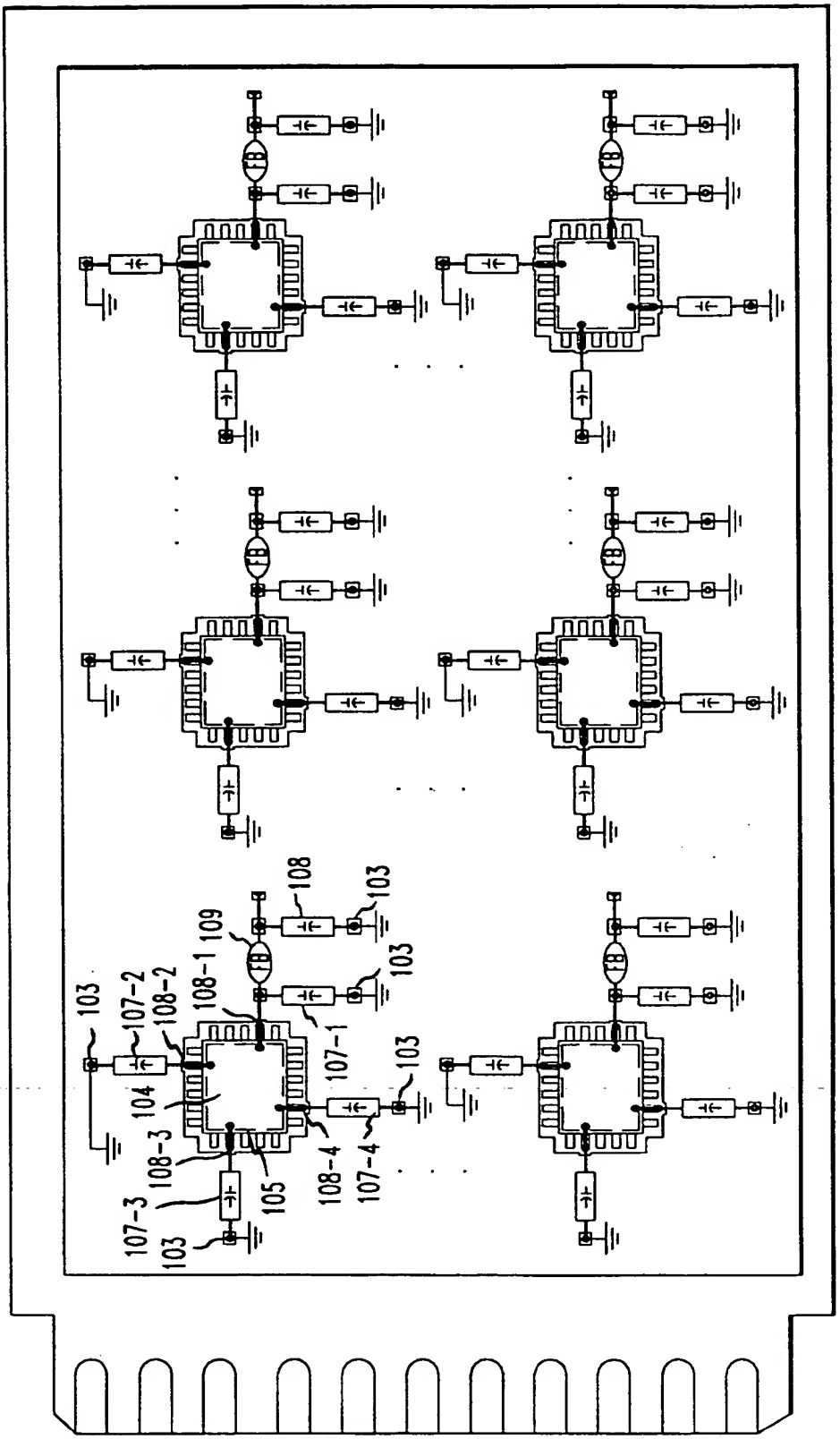


FIG. 3

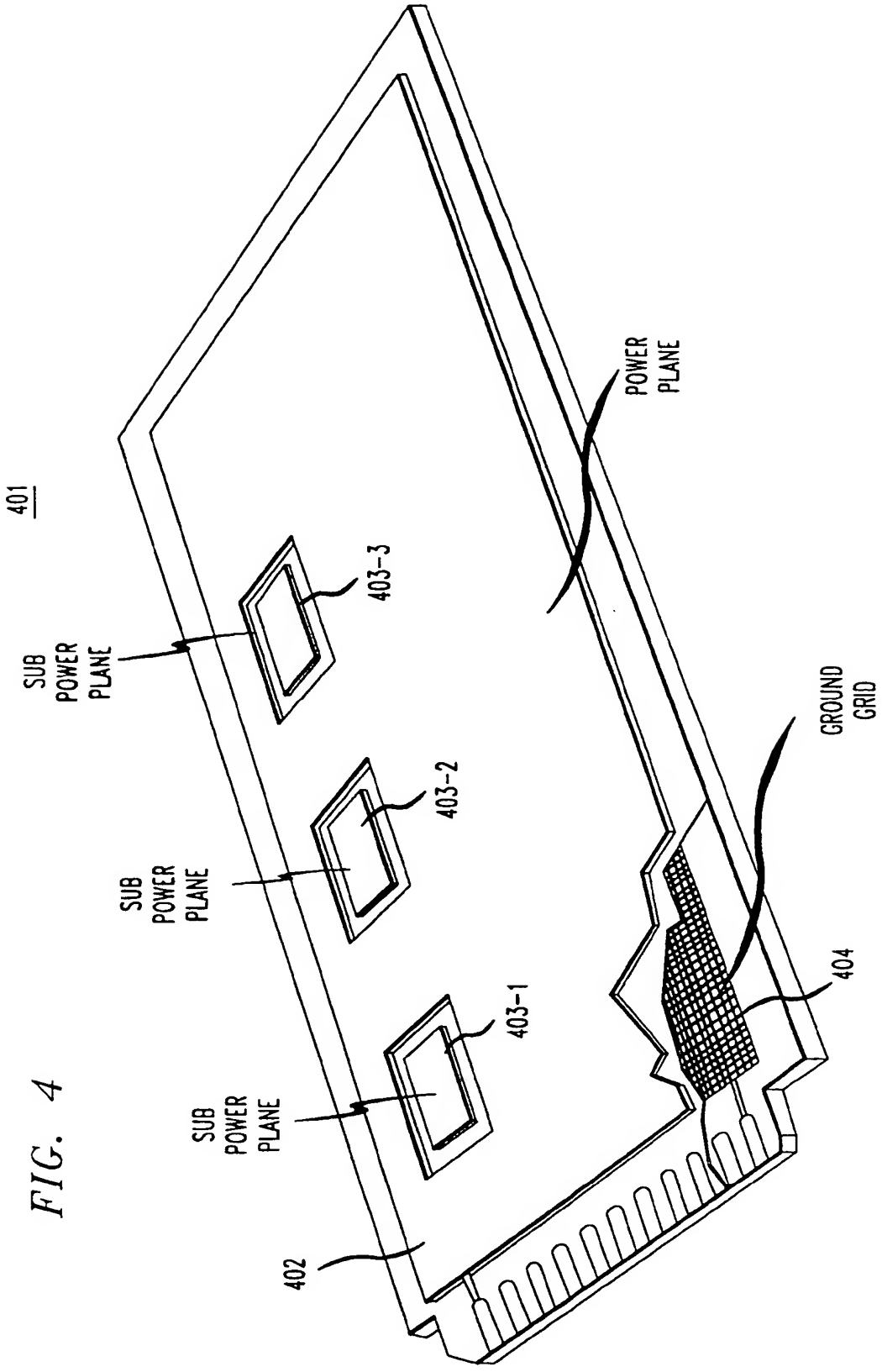


FIG. 4

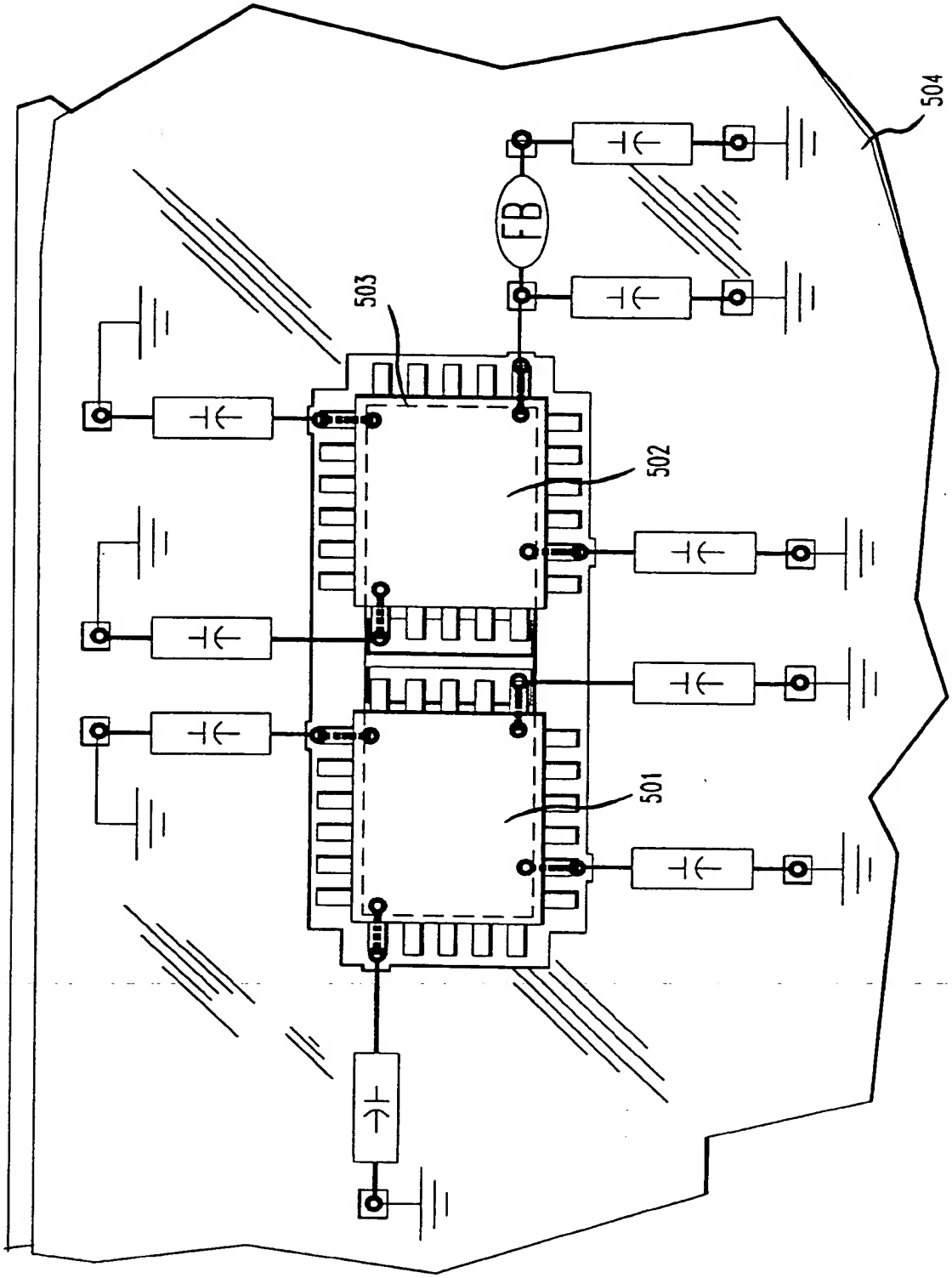


FIG. 5

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 91 30 7133

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	DE-A-3 626 151 (SIEMENS) * the whole document * ---	1	H05K9/00
A	NEW ELECTRONICS. INCORPORATING ELECTRONICS TODAY. February 1989, LONDON GB pages 56 - 57; 'CONNECTING TO BOARD PARTITION STANDARD' * the whole document * ---	1	
A	GB-A-917 514 (SANDERS ASSOCIATED INC) * the whole document * ---	7	
P,X	US-A-5 023 753 (ABE) * the whole document * -----	1-3	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H05K
H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 NOVEMBER 1991	TOUSSAINT

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